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EXAMINER	
NGUYEN, MINH T	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/921,561	Applicant(s) KOMURA ET AL.	
	Examiner Minh Nguyen	Art Unit 2816	H

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicants' amendment filed on 6/13/03 has been received and entered in the case. The amendment to the specification which requires the interpretation of the recited means in the claims to the structures shown in the drawings overcome the prior art rejections in the previous Office Action. However, new grounds of rejections to the claims and the newly added claims are set forth below. This action is FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4, 6-7, 9-13, 16-18, 26-27, 29-30, 32, 34 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,778,214, issued to Taya et al.

As per claim 1, Taya discloses a delay circuit (Fig. 12) comprising:

a delay section having two or more delay stages (11a, 11b, ...), adding predetermined delay times to an input signal (at the signal input terminal); and

selecting switch sections (12a, 12b, ...) wherein

the selecting switch section 12a (see Fig. 13B for details) comprises:

a buffer section (FETs 125 and 128);

a selecting section means (FETs 126 and 127) directly connected to the buffer section for activating the buffer section to establish a delay path (met because the structure of the Taya's selecting switch section is *exactly* the same as the structure of the present invention selecting switch section shown in Fig. 4) to the output (the signal output terminal).

As per claim 2, the recited connections are shown in Fig. 12, and output terminals of the selecting switch sections (12a, 12b, ...) are mutually joined (at the input of the buffer 15).

As per claim 4, the recited first transistor reads on FET 125 having gate receives the (SW INPUT) signal, the recited second transistor reads on FET 126 having gate receives the control signal (SELECTION SIGNAL), FETs 125 and 126 are directly connected in series (as shown) between the output terminal (SW OUTPUT) and the first power supply voltage (REFERENCE POTENTIAL).

As per claim 6, the first transistor 125 is connected between the second transistor 126 and the first power supply voltage (REFERENCE POTENTIAL).

As per claim 7, the recited third and fourth transistors read on FETs 128 and 127, respectively.

As per claim 9, shown in Fig. 13B, FETs 126 and 127 are connected as recited.

As per claim 10, the upper REFERECE POTENTIAL is clearly a power supply potential, and FETs 125 and 126 are clearly PMOSs.

As per claim 11, when FETs 128 and 127 are seen as first and second transistors and the lower REFERENCE POTENTIAL is the first power supply potential, the recited limitations are met.

As per claim 12, when FETs 125 and 126 are seen as third and fourth transistors and the upper REFERENCE POTENTIAL is the second power supply potential, the recited limitations are met.

As per claim 13, met for the same reasons noted in claim 11.

As per claim 16, delay stages 11a, 11b, ... are connected as recited.

As per claim 18, the recited limitation substantial uniform rise delay time and fall delay time" is inherently met since Taya delay stages are CMOS inverters (column 9, lines 40-43).

As per claim 26, rejected for the same reasons noted in claim 1.

As per claim 27, rejected for the same reasons noted in claim 4.

As per claims 29-30, these claims are merely methods to operate a delay circuit having the structure shown in Fig. 4, since Taya teaches the structure, he inherently teaches the recited methods.

As per claim 32, rejected for the same reasons noted in claim 1, the recited limitation "substantial uniform rise delay time and fall delay time" is inherently met since Taya delay stages are CMOS inverters (column 9, lines 40-43).

As per claim 17, the recited structure is shown in Fig. 12.

As per claim 34, rejected for the same reasons noted in claim 1, and further, the recited first and second transistors read on FETs 125 and 126, respectively.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 8, 14-15, 19-25, 28, 31 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,778,214, issued to Taya et al.

As per claim 5, Taya disclose a delay circuit having details discussed in claim 4 above, and further, the arrangement of the first and second transistors is the same as the one called for in claim 6. Claim 5 calls for another arrangement of the first and second transistors which is not explicitly taught by Taya, i.e., different species.

However, changing the position of the first and second transistors in the Taya delay circuit is seen as an obvious modification by an average person skilled in the art.

The Examiner takes Official Notice the fact that arranging the locations of elements in an integrated circuit is a well-known practice to reduce EMI problems.

It would have been obvious to one skilled in the art at the time of the invention was made to switch the position of the Taya first and second transistors, the advantage and motivation would be to reduce potential EMI problems.

The Examiner further notes that if the Applicants strongly believe that the structure of claim 5 and 6 are distinct and they are not an obvious modification, it may be appropriate to require the Applicants to elect a single species for examination.

As per claim 8, rejected for the same reason and motivation as discussed in claim 5.

As per claim 14, Taya discloses the delay circuit as discussed in claim 4 but does not explicitly disclose the drive capacity of the second transistor is larger than the drive capacity of the first transistor.

However, this limitation is seen as an obvious modification by a person skilled in the art at the time of the invention was made for improving the accuracy of the delay time, since the second transistor is used as a switch in the delay circuit, the larger the drive capacity of the second transistor reduces the delay time contributed by the second transistor.

As per claim 15, rejected for the same reason and motivation as discussed in claim 14.

As per claim 19, Taya discloses the delay circuit as discussed in claim 18 above but he does not explicitly disclose that each of the delay stages is implemented using even basis units connected in series as called for in the claim.

The examiner takes Official Notice the fact that it is old and well-known in the art to use inverters connected in series as a delay stage, and each of the inverters is counted as a basis unit delay, two inverters can be connected in series to implement a delay stage in a delay circuit so that the rise and fall times of an input signal are balanced.

It would have been obvious to one skilled in the art at the time of the invention was made to use two inverters connected in series to implement each of the Taya delay stages.

The motivation/suggestion for doing so would have to obtain a balanced rise and fall time of the output signal when the signal is delayed by the Taya's delay circuit.

As per claim 20, the modification discussed in claim 19 clearly discloses the logic inversion sections are inverter gates.

As per claim 21, this claim is rejected for the same reasons noted in claim 19.

As per claim 24, Taya discloses the delay circuit as discussed in claim 16 above but he does not explicitly disclose that each of the delay stages having the same structure.

The examiner takes Official Notice the fact that using the same structure to implement each of the delay stages has the advantage of cost reducing since they are able to mass production.

It would have been obvious to one skilled in the art at the time of the invention was made to implement the Taya delay stages using the same structure for the advantage of minimizing the cost.

As per claims 22 and 23, the combination discussed in claim 21 above discloses the delay circuit includes predetermined delay stages wherein each of the delay stage is implemented using two inverters connected in series but he does not explicitly disclose that each of the delay stages is implemented using NAND gates to function as inverters by connecting one of its input terminal to VDD as called for in claim 22 or each of the delay stages is implemented using NOR gates to function as inverters by connecting one of its input terminal to ground as called for in claim 23.

The examiner takes Official Notice the fact that an NAND gate with one of its input terminals connected to VDD or a NOR gate with one of its input terminals connected to ground is art recognized equivalent to an inverter since it is functioned as an inverter.

It would have been obvious to replace the inverters used to implement the delay stages in the combination discussed in claim 21 with NAND gates or NOR gates.

The suggestion/motivation for doing so would have been obvious since during the assembly process of the Taya circuit, a worker would be motivated to replace the inverter in the Taya delay stage by a NAND gate or NOR gate when the inverter is not readily available, and therefore, time for waiting the parts is saved.

As per claim 25, another species, rejected for the same reasons and motivations as discussed in claim 5.

As per claims 28 and 31, these claims are rejected for the same reasons noted in claim 18.

As per claim 33, rejected for the same reasons noted in claim 5.

Response to Arguments

4. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

9/12/03

Minh Nguyen
Primary Examiner
Art Unit 2816